Amendments to the Claims:

Claims 1-37 (Canceled).

38. (Currently Amended): Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least a single well formed therein, the well comprising a base of said insulative layer received over the word lines, the insulative layer within which said well is formed peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, ~~the~~ said insulative layer of the well having a substantially planar base;

a plurality of memory cell storage capacitors received within said single well, the memory cell storage capacitors respectively comprising a storage ~~node container which is~~ node, the storage node comprising a portion having a container shape, said container-shaped portion being received partially within the insulative layer through the ~~well~~ insulative layer base of the well ~~over the word lines~~; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

39. (Original): The memory circuitry of claim 38 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

40. (Original): The memory circuitry of claim 38 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

41. (Original): The memory circuitry of claim 38 comprising buried digit lines; the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

42. (Currently Amended): Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

digit lines received over the word lines;

an insulative layer received over the word lines, the digit lines and the substrate, the insulative layer having at least a single well formed therein, the well comprising a base of said insulative layer received over the word lines and the digit lines, the insulative layer within which said well is formed peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, an oxygen diffusion barrier layer received over the ~~well~~ insulative layer base of the well;

a plurality of memory cell storage capacitors received within said single well over the word lines and the digit lines, the memory cell storage capacitors respectively comprising a storage node ~~container~~ which is received within the insulative layer through the oxygen diffusion barrier layer and through the ~~well~~ insulative layer base of the well; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

43. (Original): The memory circuitry of claim 42 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

44. (Original): The memory circuitry of claim 42 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

Claims 45-47 (Canceled).

48. (Previously Presented): The memory circuitry of claim 38 wherein the oxygen diffusion barrier layer received over the well base comprises Si_3N_4.

49. (Previously Presented): The memory circuitry of claim 48 wherein the Si_3N_4-comprising layer has a thickness of from about 40 Angstroms to about 125 Angstroms.

50. (Previously Presented): The memory circuitry of claim 48 wherein the Si_3N_4-comprising layer has a thickness of from about 50 Angstroms to about 70 Angstroms.

51. (Previously Presented): The memory circuitry of claim 48 wherein the insulative layer comprises SiO_2.

52. (Previously Presented): The memory circuitry of claim 51 wherein the Si_3N_4-comprising layer has a thickness of from about 40 Angstroms to about 125 Angstroms.

53. (Previously Presented): The memory circuitry of claim 51 wherein the Si_3N_4-comprising layer has a thickness of from about 50 Angstroms to about 70 Angstroms.

54. (Previously Presented): The memory circuitry of claim 38 wherein one of the storage node electrodes is spaced laterally inward of the outline peripherally defined by the well thereby forming a space between said one electrode and said outline.

55. (Previously Presented): The memory circuitry of claim 42 wherein the one of the storage node electrode is spaced laterally inward of the outline peripherally defined by the well thereby forming a space between said one electrode and said outline.

56. (Previously Presented): The memory circuitry of claim 42 wherein the base is substantially planar.

57. (Previously Presented): The memory circuitry of claim 42 wherein the insulative layer is formed to have a substantially planar outermost surface, the memory cell storage capacitors respectively comprising an outer cell electrode having a topmost surface which is received elevationally outward of the insulative layer.

58. (Previously Presented): The memory circuitry of claim 42 wherein the Si_3N_4-comprising oxygen diffusion barrier layer is received on the well base.

59. (New): The memory circuitry of claim 42 wherein the storage node comprises a portion having a container shape, said container-shaped portion being received partially within the insulative layer through the insulative layer base of the well.